IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No.: **RA001C13**)

In the Application of:	)
	)
FARMWALD ET AL.	)
	)
Serial No: Continuation of 09/835,263	)
	)
Filed: Herewith	)
	)
Title: SYNCHRONOUS INTEGRATED CIRCUIT DEVICE (As Amended)	)

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the examination of the above-referenced application, kindly amend the application as follows:

IN THE ABSTRACT:

Please delete the Abstract of the Disclosure and substitute the attached Abstract of the Disclosure.

IN THE TITLE:

Please delete the title and substitute:

SYNCHRONOUS INTEGRATED CIRCUIT DEVICE

IN THE SPECIFICATION:

(A marked-up version of the following amendments to the Specification is enclosed herewith)

On page 1, line 8, **insert**:

This application is a continuation of Application No. 09/835,263, filed on April 13, 2001 (still pending), which is a continuation of Application No. 09/545,648, filed on April 10, 2000 (still pending), which is a continuation of Application No. 09/161,090, filed on September 25, 1998 (now U.S. Patent 6,049,846), which is a division of Application No. 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580), which is a division of Application No. 08/448,657, filed May 24, 1995 (now U.S. Patent 5,638,334), which is a division of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327), which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755), which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).

On page 3, **substitute** the paragraph starting on line 6 with the following paragraph:

Prior art memory systems have attempted to solve the problem of high speed access to memory with limited success. U.S. Pat. No. 3,821,715 (Hoff et.al.), was issued to Intel Corporation for the earliest 4-bit microprocessor. That patent describes a bus connecting a single central processing unit (CPU) with multiple RAMs and ROMs. That bus multiplexes addresses and data over a 4-bit wide bus and uses point-to-point control signals to select particular RAMs or ROMs. The access time is fixed and only a single processing element in permitted. There is no block-mode type of operation, and most important, not all of the interface signals between the devices are bused (the ROM and RAM control lines and the RAM select lines are point-to-point).

On page 6, **substitute** the paragraph starting on line 1, with the following paragraph:

In U.S. Pat. No. 4,646,270 (Voss), a video RAM is described which implements a parallel-load, serial-out shift register on the output of a DRAM. This generally allows greatly improved bandwidth (and has been extended to 2, 4 and greater width shift-out paths.) The rest of the interfaces to the DRAM (RAS, CAS, multiplexed address, etc.) remain the same as for conventional DRAMS.

On page 10, **substitute** the paragraphs starting on lines 18 and 21, with the following two paragraphs, respectively:

FIGS. 7a and 7b show the timing whereby signals from two devices can overlap temporarily and drive the bus at the same time.

FIGS. 8a and 8b show the connection and timing between bus clocks and devices on the bus.

On page 34, **substitute** the paragraph starting on line 4, with the following paragraph:

Slave devices do not need to detect a collision directly, but they must wait to do anything irrecoverable until the last byte (byte 5) is read to ensure that the packet is valid. A request packet with Master[0:3] equal to 0 (a retry signal) is ignored and does not cause a collision. The subsequent bytes of such a packet are ignored.

Please **substitute** the paragraph starting on page 40, line 19, and ending on page 41, line 16, with the following paragraph:

In a preferred embodiment, a standard data block size can be selected for use with ECC, and the ECC method will determine the required number of bits of information in a corresponding ECC block. RAMs containing ECC information can be programmed to store an access time that in equal to: (1) the access time of the normal RAM (containing data) plus the time to access a standard data block (for corrected data) minus the time to send a request packet (6 bytes); or (2) the access time of a normal RAM minus the time to access a standard ECC block minus the time to send a request packet. To read a data block and the corresponding ECC block, the master simply issues a request for the data immediately followed by a request for the ECC block. The ECC RAM will wait for the selected access time then drive its data onto the bus right after (in case (1) above)) the data RAM has finished driving out the data block. Persons skilled in the art will recognize that the access time described in case (2) above can be used to drive ECC data before the data is driven onto the bus lines and will recognize that writing data can be done by analogy with the method described for a

read. Persons skilled in the art will also recognize the adjustments that must be made in the bus-busy structure and the request packet arbitration methods of this invention in order to accommodate these paired ECC requests.

Please **substitute** the paragraph starting on page 45, line 17, and ending on page 46, line 17, with the following:

Referring to FIGS. 7a and 7b, although there is no stable condition where two devices drive the bus at the same time, conditions can arise because of propagation delay on the wires where one device, A 41, can start driving its part of the bus 44 while the bus is still being driven by another device, B 42 (already asserting a logical 1 on the bus). In a system using current drivers, when B 42 is driving the bus (before time 46), the value at points 44 and 45 is logical 1. If B 42 switches off at time 46 just when A 41 switches on, the additional drive by device A 41 causes the voltage at the output 44 of A 41 to briefly below the normal value. The voltage returns to its normal value at time 47 when the effect of device B 42 turning off is felt. The voltage at point 45 goes to logical 0 when device B 42 turns off, then drops at time 47 when the effect of device A 41 turning on is felt. Since the logical 1 driven by current from device A 41 is propagated irrespective of the previous value on the bus, the value on the bus is guaranteed to settle after one time of flight (t_f) delay, that is, the time it takes a signal to propagate from one end of the bus to the other. If a voltage drive was used (as in ECL wired-ORing), a logical 1 on the bus (from device B 42 being previously driven) would prevent the transition put out by device A 41 being felt at the most remote part of the system, e.g., device 43, until the turnoff waveform from device B 42 reached device A 41 plus one time of flight delay, giving a worst case settling time of twice the time of flight delay.

Please **substitute** the paragraph starting on page 46, line 20, and ending on page 47, line 12, with the following paragraph:

Clocking a high speed bus accurately without introducing error due to propagation delays can be implemented by having each device monitor two bus clock signals and then derive internally a device clock, the true system clock. The bus clock information can be sent on one or two lines to provide a mechanism for each bused

device to generate an internal device clock with zero skew relative to all the other device clocks. Referring to FIG. 8a, in the preferred implementation, a bus clock generator 50 at one end of the bus propagates an early bus clock signal in one direction along the bus, for example on line 53 from right to left, to the far end of the bus. The same clock signal then is passed through the direct connection shown to a second line 54, and returns as a late bus clock signal along the bus from the far and to the origin, propagating from left to right. A single bus clock line can be used if it is left unterminated at the far end of the bus, allowing the early bus clock signal to reflect back along the same line as a late bus clock signal.

Please **substitute** the paragraph starting on page 49, line 12, and ending on page 50, line 3, with the following paragraph:

Referring to FIG. 9, each primary bus unit can be mounted on a single circuit board 66, sometimes called a memory stick. Each transceiver device 19 in turn connects to a transceiver bus 65, similar or identical in electrical and other respects to the primary bus 18 described at length above. In a preferred implementation, all masters are situated on the transceiver bus so there are no transceiver delays between masters and all memory devices are on primary bus units so that all memory accesses experience an equivalent transceiver delay, but persons skilled in the art will recognize how to implement systems which have masters on more than one bus unit and memory devices on the transceiver bus as well as on primary bus units. In general, each teaching of this invention which refers to a memory device can be practiced using a transceiver device and one or more memory devices on an attached primary bus unit. Other devices, generically referred to as peripheral devices, including disk controllers, video controllers or I/O devices can also be attached to either the transceiver bus or a primary bus unit, as desired. Persons skilled in the art will recognize how to use a single primary bus unit or multiple primary bus units as needed with a transceiver bus in certain system designs.

Please **substitute** the paragraph starting on page 53, line 24, and ending on page 54, line 22, with the following paragraph:

A block diagram of the preferred input/output circuit for address/data/control lines is shown in FIG. 10. This circuitry is particularly well-suited for use in DRAM devices but it can be used or modified by one skilled in the art for use in other devices connected to the bus of this invention. It consists of a set of input receivers 71, 72 and output driver 76 connected to input/output line 69 and pad 75 and circuitry to use the internal clock 73 and internal clock complement 74 to drive the input interface. The clocked input receivers take advantage of the synchronous nature of the bus. To further reduce the performance requirements for device input receivers, each device pin, and thus each bus line, is connected to two clocked receivers, one to sample the even cycle inputs, the other to sample the odd cycle inputs. By thus de-multiplexing the input 69 at the pin, each clocked amplifier is given a full 2 ns cycle to amplify the bus low-voltage-swing signal into a full value CMOS logic signal. Persons skilled in the art will recognize that additional clocked input receivers can be used within the teachings of this invention. For example, four input receivers could be connected to each device pin and clocked by a modified internal device clock to transfer sequential bits from the bus to internal device circuits, allowing still higher external bus speeds or still longer settling times to amplify the bus low-voltage-swing signal into a full value CMOS logic signal.

Please **substitute** the paragraph starting on page 58, line 13, and ending on 59, line 2, with the following paragraph:

In the preferred embodiment, two sets of these delay lines are used, one to generate the true value of the internal device clock 73, and the other to generate the complement 74 without adding any inverter delay. The dual circuit allows generation of truly complementary clocks, with extremely small skew. The complement internal device clock is used to clock the `event` input receivers to sample at time 127, while the true internal device clock is used to clock the `odd` input receivers to sample at time 125. The true and complement internal device clocks 73 and 74 are also used to select which data is driven to the output drivers. The gate delay between the internal device

clock and output circuits driving the bus is slightly greater than the corresponding delay for the input circuits, which means that the new data always will be driven on the bus slightly after the old data has been sampled.

Please **substitute** the paragraph starting on page 60, line 1, and ending on page 61, line 8, with the following paragraph:

Running the internal I/O lines in the conventional way at high bus cycle rates is not possible. In the preferred method, several (preferably 4) bytes are read or written during each cycle and the column access path is modified to ran at a lower rate (the inverse of the number of bytes accessed per cycle, preferably 1/4 of the bus cycle rate). Three different techniques are used to provide the additional internal I/O lines required and to supply data to memory cells at this rate. First, the number of I/O bit lines in each subarray running through the column decoder 147 A, B is increased, for example, to 16, eight for each of the two columns of column sense amps and the column decoder selects one set of columns from the "top" half 148 of subarray 150 and one set of columns from the "bottom" half 149 during each cycle, where the column decoder selects one column sense amp per I/O bit line. Second, each column I/O line is divided into two halves, carrying data independently over separate internal I/O lines from the left half 147A and right half 147B of each subarray (dividing each subarray into quadrants) and the column decoder selects sense amps from each right and left half of the subarray, doubling the number of bits available at each cycle. Thus each column decode selection turns on n column sense amps, where n equals four (top left and right, bottom left and right quadrants) times the number of I/O lines in the bus to each subarray quadrant (8 lines each times 4=32 lines in the preferred implementation). Finally, during each RAS cycle, two different subarrays, e.g. 157 and 153, are accessed. This doubles again the available number of I/O lines containing data. Taken together, these changes increase the internal I/O bandwidth by at least a factor of 8. Four internal buses are used to route these internal I/O lines. Increasing the number of I/O lines and then splitting them in the middle greatly reduces the capacitance of each internal I/O line which in turn reduces the column access time, increasing the column access bandwidth even further.

IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

Kindly **add** the following claims:

151. A controller device for controlling a synchronous dynamic random access memory device, the controller device comprises:

first output driver circuitry to output block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device; and

input receiver circuitry to receive the amount of data output by the memory device.

152. The controller device of claim 151 further including second output driver circuitry to output an operation code to the memory device, wherein the operation code specifies a read operation and, in response to the operation code, the memory device outputs the amount of data.

153. The controller device of claim 152 wherein the operation code is included in a packet.

154. The controller device of claim 153 wherein the block size information and the operation code are included in the same packet.

155. The controller device of claim 152 wherein the first output driver circuitry outputs the block size information in response to a first transition of an external clock signal and the second output driver circuitry outputs the operation code in response to a second transition of the external clock signal.

156. The controller device of claim 152 wherein the first output driver circuitry and the second output driver circuitry output address information to the memory device.

157. The controller device of claim 156 wherein the block size information, the address information and the operation code are output to the memory device via an external bus.

158. The controller device of claim 157 wherein the external bus includes a plurality of signal lines to carry, in a multiplexed format, the block size information, the operation code and the address information.

159. The controller device of claim 151 further including delay locked loop circuitry, coupled to the input receiver circuitry, to generate an internal clock signal, wherein the input receiver circuitry samples the amount of data in response to the internal clock signal.

160. The controller device of claim 151 further including delay locked loop circuitry, coupled to the first output driver circuitry, to generate an internal clock signal, wherein the first output driver circuitry outputs the block size information in response to the internal clock signal.

161. The controller device of claim 151 wherein the block size information is a binary code.

162. The controller device of claim 151 wherein the input receiver circuitry samples:

a first portion of the amount of data during a first half of a clock cycle of the external clock signal; and

a second portion of the amount of data during a second half of the clock cycle of the external clock signal.

163. The controller device of claim 151 wherein the input receiver circuitry samples:

a first portion of the amount of data in response to a rising edge of the external clock signal; and

a second portion of the amount of data in response to a falling edge of the external clock signal.

164. An integrated circuit device comprising:

a plurality of output drivers to output block size information to a second integrated circuit device, wherein the block size information represents an amount of data to be output by the second integrated circuit device;

a delay locked loop to generate an internal clock signal; and

a plurality of input receivers, coupled to the delay locked loop, to sample the amount of data output by the second integrated circuit device, wherein the amount of data is sampled synchronously with respect to the internal clock signal.

165. The integrated circuit device of claim 164 further including a clock receiver to receive an external clock signal wherein the delay locked loop generates the internal clock signal using the external clock signal.

166. The integrated circuit device of claim 164 wherein the output drivers output the block size information to the second integrated circuit device via a bus, wherein the bus includes a plurality of signal lines.

167. The integrated circuit device of claim 166 wherein the plurality of signal lines carry, in a multiplexed format, an operation code, address information and the block size information.

168. The integrated circuit device of claim 164 wherein the block size information is a binary code.

169. The integrated circuit device of claim 164 wherein the block size information is included in a request packet.

170. The integrated circuit device of claim 169 wherein the amount of data output by the second integrated circuit device is included in a data packet.

171. The integrated circuit device of claim 170 wherein the data packet is output by the second integrated circuit device onto a set of signal lines, and the request packet is output to the second integrated circuit device via the same set of signal lines.

172. The integrated circuit device of claim 164 wherein:

during a first half of a clock cycle of the external clock signal, the plurality of input receivers sample a first portion of the amount of data output by the second integrated circuit device; and

during a second half of the clock cycle of the external clock signal, the plurality of input receivers sample a second portion of the amount of data output by the second integrated circuit device.

173. The integrated circuit device of claim 164 wherein:

the plurality of input receivers sample a first portion of the amount of data output by the second integrated circuit device in response to a rising edge of the external clock signal; and

the plurality of input receivers sample a second portion of the amount of data output by the second integrated circuit device in response to a falling edge of the external clock signal.

174. An integrated circuit device for controlling a synchronous memory device, the controller integrated circuit comprises:

clock receiver circuitry to receive an external clock signal;

delay locked loop circuitry, coupled to the clock receiver circuitry, to generate an internal clock signal; and

a first plurality of output drivers, coupled to the delay locked loop circuitry, to output an amount of data in response to the internal clock signal.

175. The integrated circuit device of claim 174 further including input receivers to sample data that is output by the memory device.

176. The integrated circuit device of claim 175 wherein the input receivers are coupled to the delay locked loop circuitry to sample the data in response to the internal clock signal.

177. The integrated circuit device of claim 174 wherein:

on a rising edge transition of the external clock signal, the input receivers sample a first portion of the data that is output by the memory device; and

on a falling edge transition of the external clock signal, the input receivers sample a second portion of the data that is output by the memory device.

178. The integrated circuit device of claim 174 further including a second plurality of output drivers to output a first operation code to the memory device, wherein the first operation code specifies a read operation, and wherein the memory device, in response to the first operation code, outputs data.

179. The integrated circuit device of claim 174 wherein:

the first plurality of output drivers output a first portion of the amount of data in response to a rising edge transition of the external clock signal; and

the first plurality of output drivers output a second portion of the amount of data in response to a falling edge transition of the external clock signal.

180. The integrated circuit device of claim 174 further including a second plurality of output drivers to output a second operation code to the synchronous memory device, wherein the second operation code specifies a write operation, and wherein the memory device, in response to the second operation code, samples the amount of data.

181. The integrated circuit device of claim 174 wherein the first plurality of output drivers are coupled to the memory device via an external bus that includes a plurality of signal lines.

182. The integrated circuit device of claim 181 wherein the first plurality of output drivers output an operation code and address information to the memory device, in a multiplexed format, via the plurality of signal lines.

183. The integrated circuit device of claim 174 wherein the first plurality of output drivers include a plurality of output drivers to output an operation code to the memory device, wherein the operation code specifies a read operation, and wherein the memory device outputs data in response to the operation code specifying the read operation.

184. An integrated circuit controller device for controlling a synchronous dynamic random access memory device, the controller device comprises:

a first plurality of output drivers to output block size information to the memory device, wherein the block size information represents an amount of data to be output by the memory device;

a second plurality of output drivers to output an operation code to the memory device, wherein the operation code specifies a read operation, and wherein the memory device outputs the amount of data to the controller device in response to the operation code; and

a plurality of input receivers to receive the amount of data output by the memory device.

185. The controller device of claim 184 wherein the operation code is included in a packet.

186. The controller device of claim 185 wherein the block size information and the operation code are included in the same packet.

187. The controller device of claim 184 wherein the block size information is output in response to a first transition of an external clock signal and the operation code is output in response to a second transition of the external clock signal.

188. The controller device of claim 184 wherein both the first plurality of output drivers and the second plurality of output drivers output address information to the memory device.

189. The controller device of claim 188 wherein the block size information, the operation code, and the address information are output, in a multiplexed format, to the memory device via an external bus.

190. The controller device of claim 184 further including a clock receiver to receive an external clock signal, wherein the first plurality of output drivers outputs the block size information synchronously with respect to the external clock signal.

191. The controller device of claim 190 further including a delay locked loop coupled to the clock receiver and the plurality of input receivers, wherein the delay locked loop generates an internal clock signal, and wherein the plurality of input receivers sample the amount of data in response to the internal clock signal.

192. The controller device of claim 190 further including a delay locked loop coupled to the first plurality of output drivers and the clock receiver, wherein the delay locked loop generates an internal clock signal, and wherein the first plurality of output drivers circuitry outputs the block size information in response to the internal clock signal.

193. The controller device of claim 184 wherein the block size information is a binary code.

194. The controller device of claim 184 wherein:

the plurality of input receivers samples a first portion of the amount of data during a first half of a clock cycle of the external clock signal; and

the plurality of input receivers samples a second portion of the amount of data during a second half of the clock cycle of the external clock signal.

REMARKS

This Preliminary Amendment seeks to place this application in condition for allowance. This application is a continuation of Application Serial No. 09/835,263 which is a continuation of Application Serial No. 09/545,648. Application Serial No. 09/835,263 is pending.

REQUEST FOR PRIORITY

Applicants request priority to Application Serial No. 07/510,898, filed April 18, 1990, now abandoned. Applicants request such priority through Application No. 09/835,263, filed on April 13, 2001 (still pending), which is a continuation of Application No. 09/545,648, filed on April 10, 2000 (still pending), which is a continuation of Application No. 09/161,090, filed on September 25, 1998 (now U.S. Patent 6,049,846), which is a division of Application No. 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580), which is a division of Application No. 08/448,657, filed May 24, 1995 (now U.S. Patent 5,638,334), which is a division of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327), which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755), which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).

Accordingly, Applicants claim the benefit of the filing date of Application Serial No. 07/510,898 -- i.e., April 18, 1990. The specification has been amended to identify the continuation/divisional or related U.S. application data identified above. No new matter has been added.

AMENDMENTS TO THE CLAIMS

In this continuation application, Applicants present new claims which set forth novel and unobvious features of Applicants' invention. Applicants submit new claims 151-194 to more fully claim the Applicants invention. No new matter has been added.

The newly submitted claims are believed to be fully supported by the specification -- see, for example, Figures 1, 2, 4 and 10-13, and 15; page 13, lines 13-17; page 20, line 14 to page 21, line 20; page 22, line 11 to page 25, line 8; page 27, line 1 to page 28, line 20; page 46, line 19 to page 48, line 17; page 53, line 23 to page

59, line 2; page 71, line 20 to page 72, line 21; page 73, lines 20 to page 74, line 31; and page 115, lines 10-22.

AMENDMENTS TO THE SPECIFICATION

Applicants have also amended the specification to include the priority data, and to correct obvious spelling, typographical and grammatical errors. No new matter has been added.

AMENDMENTS TO THE ABSTRACT

A new Abstract of the Disclosure is attached hereto. No new matter has been added.

DRAWING CHANGES

Accompanying this Preliminary Amendment is a Request to Approve Drawing Changes. Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, in particular, page 55, lines 12-16 and page 58, lines 13-23. The proposed changes are indicated in red. No new matter has been added. Applicants respectfully request that the Examiner approve the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached to the Request.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

Respectfully submitted,

Date: Dec 21/01

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ABSTRACT OF THE DISCLOSURE

A controller device for controlling a synchronous dynamic random access memory device. The controller device includes output driver circuitry to output block size information to the memory device. The block size information defines an amount of data to be output by the memory device. In addition, the controller device includes input receiver circuitry to receive the amount of data output by the memory device.

Version With Markings to show Changes made to the Specification

On page 3, starting on line 6:

Prior art memory systems have attempted to solve the problem of high speed access to memory with limited success. U.S. Pat. No. 3,821,715 (Hoff et.al.), was issued to Intel Corporation for the earliest 4-bit [micro-processor] microprocessor. That patent describes a bus connecting a single central processing unit (CPU) with multiple RAMs and ROMs. That bus multiplexes addresses and data over a 4-bit wide bus and uses point-to-point control signals to select particular RAMs or ROMs. The access time is fixed and only a single processing element in permitted. There is no block-mode type of operation, and most important, not all of the interface signals between the devices are bused (the ROM and RAM control lines and the RAM select lines are point-to-point).

On page 6, starting on line 1:

In U.S. Pat. No. 4,646,270 [4,646,279](Voss), a video RAM is described which implements a parallel-load, serial-out shift register on the output of a DRAM. This generally allows greatly improved bandwidth (and has been extended to 2, 4 and greater width shift-out paths.) The rest of the interfaces to the DRAM (RAS, CAS, multiplexed address, etc.) remain the same as for conventional DRAMS.

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[Figure 7 shows] FIGS. 7a and 7b show the timing whereby signals from two devices can overlap temporarily and drive the bus at the same time.

[Figure 8 shows] FIGS. 8a and 8b show the connection and timing between bus clocks and devices on the bus.

On page 34, starting on line 4:

Slave devices do not need to detect a collision directly, but they must wait to do anything irrecoverable until the last byte (byte 5) is read to ensure that the packet is valid. A request packet with Master[0:3] equal to 0 (a retry signal) is ignored and does not cause a collision. The subsequent bytes of such a packet are ignored.

On page 40, starting on line 19:

In a preferred embodiment, a standard data block size can be selected for use with ECC, and the ECC method will determine the required number of bits of information in a corresponding ECC block. RAMs containing ECC information can be programmed to store an access time that in equal to: (1) the access time of the normal RAM (containing data) plus the time to access a standard data block (for corrected data) minus the time to send a request packet (6 bytes); [or']or (2) the access time of a normal RAM minus the time to access a standard ECC block minus the time to send a request packet. To read a data block and the corresponding ECC block, the master simply issues a request for the data immediately followed by a request for the ECC block. The ECC RAM will wait for the selected access time then drive its data onto the bus right after (in case (1) above)) the data RAM has finished driving out the data block. Persons skilled in the art will recognize that the access time described in case (2) above can be used to drive ECC data before the data is driven onto the bus lines and will recognize that writing data can be done by analogy with the method described for a read. Persons skilled in the art will also recognize the adjustments that must be made in the bus-busy structure and the request packet arbitration methods of this invention in order to accommodate these paired ECC requests.

On page 45, starting on line 17:

Referring to [Fig. 7] FIGS. 7a and 7b, although there is no stable condition where two devices drive the bus at the same time, conditions can arise because of propagation delay on the wires where one device, A 41, can start driving its

part of the bus 44 while the bus is still being driven by another device, B 42 (already asserting a logical 1 on the bus). In a system using current drivers, when B 42 is driving the bus (before time 46), the value at points 44 and 45 is logical 1. If B 42 switches off at time 46 just when A 41 switches on, the additional drive by device A 41 causes the voltage at the output 44 of A 41 to briefly below the normal value. The voltage returns to its normal value at time 47 when the effect of device B 42 turning off is felt. The voltage at point 45 goes to logical 0 when device B 42 turns off, then drops at time 47 when the effect of device A 41 turning on is felt. Since the logical 1 driven by current from device A 41 is propagated irrespective of the previous value on the bus, the value on the bus is guaranteed to settle after one time of flight (t_f) delay, that is, the time it takes a signal to propagate from one end of the bus to the other. If a voltage drive was used (as in ECL wired-ORing), a logical 1 on the bus (from device B 42 being previously driven) would prevent the transition put out by device A 41 being felt at the most remote part of the system, e.g., device 43, until the turnoff waveform from device B 42 reached device A 41 plus one time of flight delay, giving a worst case settling time of twice the time of flight delay.

On page 46, starting on line 20:

Clocking a high speed bus accurately without introducing error due to propagation delays can be implemented by having each device monitor two bus clock signals and then derive internally a device clock, the true system clock. The bus clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks. Referring to [Figure 8] FIG. 8a, in the preferred implementation, a bus clock generator 50 at one end of the bus propagates an early bus clock signal in one direction along the bus, for example on line 53 [from left to right] from right to left, to the far end of the bus. The same clock signal then is passed through the direct connection shown to a second line 54, and returns

as a late bus clock signal along the bus from the far and to the origin, propagating from [right] left to [left] right. A single bus clock line can be used if it is left unterminated at the far end of the bus, allowing the early bus clock signal to reflect back along the same line as a late bus clock signal.

On page 49, starting on line 12:

Referring to FIG. 9, each primary bus unit can be mounted on a single circuit board 66, sometimes called a memory stick. Each transceiver device 19 in turn connects to a transceiver bus 65, similar or identical in electrical and other respects to the primary bus 18 described at length above. In a preferred implementation, all masters are situated on the transceiver bus so there are no transceiver delays between masters and all memory devices are on primary bus units so that all memory accesses experience an equivalent transceiver delay, but persons skilled in the art will recognize how to implement systems which have masters on more than one bus unit and memory devices on the transceiver bus as well as on [primay] primary bus units. In general, each teaching of this invention which refers to a memory device can be practiced using a transceiver device and one or more memory devices on an attached primary bus unit. Other devices, generically referred to as peripheral devices, including disk controllers, video controllers or I/O devices can also be attached to either the transceiver bus or a primary bus unit, as desired. Persons skilled in the art will recognize how to use a single primary bus unit or multiple primary bus units as needed with a transceiver bus in certain system designs.

On page 53, starting on line 24:

A block diagram of the preferred input/output circuit for address/data/control lines is shown in FIG. 10. This circuitry is particularly well-suited for use in DRAM devices but it can be used or modified by one skilled in the art for use in other devices connected to the bus of this invention. It consists of a set of input receivers 71, 72 and output driver 76 connected to input/output line 69 and pad 75 and circuitry to use the internal clock 73 and internal clock

complement 74 to drive the input interface. The clocked input receivers take advantage of the synchronous nature of the bus. To further reduce the performance requirements for device input receivers, each device pin, and thus each bus line, is connected to two clocked receivers, one to sample the even cycle inputs, the other to sample the odd cycle inputs. By thus de-multiplexing the input [70]69 at the pin, each clocked amplifier is given a full 2 ns cycle to amplify the bus low-voltage-swing signal into a full value CMOS logic signal. Persons skilled in the art will recognize that additional clocked input receivers can be used within the teachings of this invention. For example, four input receivers could be connected to each device pin and clocked by a modified internal device clock to transfer sequential bits from the bus to internal device circuits, allowing still higher external bus speeds or still longer settling times to amplify the bus low-voltage-swing signal into a full value CMOS logic signal.

On page 58, starting on line 13:

In the preferred embodiment, two sets of these delay lines are used, one to generate the true value of the internal device clock 73, and the other to generate the complement 74 without adding any inverter delay. The dual circuit allows generation of truly complementary clocks, with extremely small skew. The complement internal device clock is used to clock the `event` input receivers to sample at time 127, while the true internal device clock is used to clock the `odd` input receivers to sample at time 125. The true and complement internal device clocks 73 and 74 are also used to select which data is driven to the output drivers. The gate delay between the internal device clock and output circuits driving the bus is slightly greater than the corresponding delay for the input circuits, which means that the new data always will be driven on the bus slightly after the old data has been sampled.

Starting on page 60, line 1:

Running the internal I/O lines in the conventional way at high bus cycle rates is not possible. In the preferred method, several (preferably 4) bytes are read or written during each cycle and the column access path is modified to ran at a lower rate (the inverse of the number of bytes accessed per cycle, preferably 1/4 of the bus cycle rate). Three different techniques are used to provide the additional internal I/O lines required and to supply data to memory cells at this rate. First, the number of I/O bit lines in each subarray running through the column decoder 147 A, B is increased, for example, to 16, eight for each of the two columns of column sense amps and the column decoder selects one set of columns from the "top" half 148 of subarray 150 and one set of columns from the "bottom" half 149 during each cycle, where the column decoder selects one column sense amp per I/O bit line. Second, each column I/O line is divided into two halves, carrying data independently over separate internal I/O lines from the left half 147A and right half 147B of each subarray (dividing each subarray into quadrants) and the column decoder selects sense amps from each right and left half of the subarray, doubling the number of bits available at each cycle. Thus each column decode selection turns on n column sense amps, where n equals four (top left and right, bottom left and right quadrants) times the number of I/O lines in the bus to each subarray quadrant (8 lines each times 4=32 lines in the preferred implementation). Finally, during each RAS cycle, two different subarrays, e.g. 157 and 153, are accessed. This doubles again the available number of I/O lines containing data. Taken together, these changes increase the internal I/O bandwidth by at least a factor of 8. Four internal buses are used to route these internal I/O lines. Increasing the number of I/O lines and then splitting them in the middle greatly reduces the capacitance of each internal I/O line which in turn reduces the column access time, increasing the column access bandwidth even further.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No.: **RA001C13**)

In the Application of:	)
	)
FARMWALD ET AL.	)
	)
Serial No: Continuation of 09/835,263	)
	)
Filed: Herewith	)
	)
Title: SYNCHRONOUS INTEGRATED CIRCUIT DEVICE (As Amended)	)

Assistant Commissioner for Patents
Washington, DC 20231

REQUEST TO APPROVE DRAWING CHANGES

Dear Sir:

Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, specifically, page 55, line 12-16 and page 58, lines 13-23. Also attached, is a photocopy of Figure 10 with the proposed changes indicated in red. No new matter has been added.

Applicants respectfully request approval of the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached hereto.

Respectfully submitted,

Date: Dec 21/01

Jose G. Moniz
Reg. No. P-50,192

Rambus Inc.
4440 El Camino Real
Los Altos, CA 94022
650-947-5336

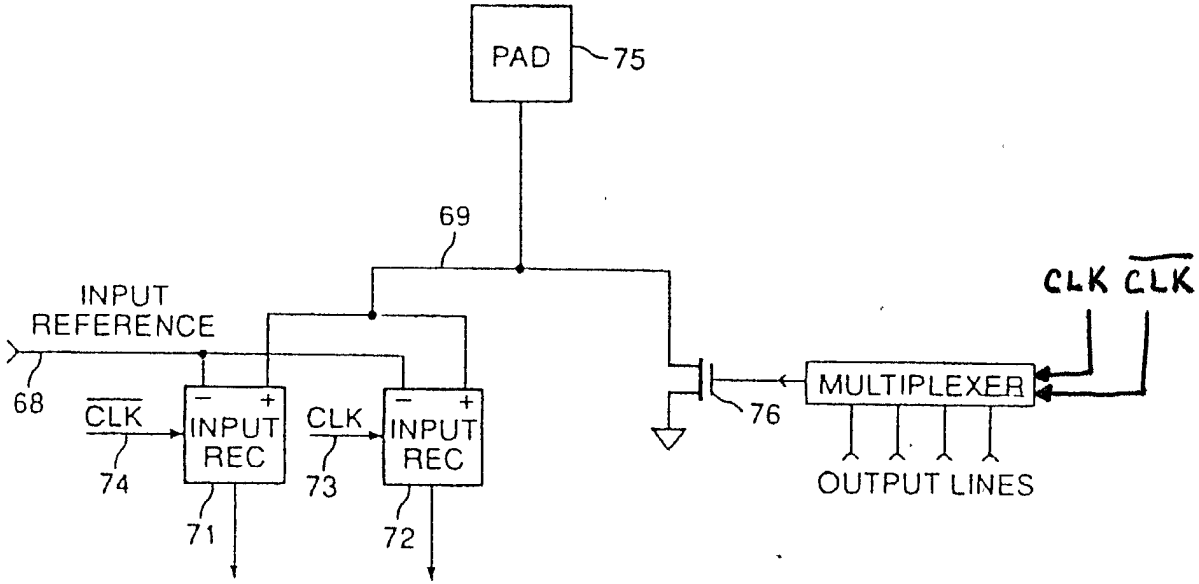

FIG. 10

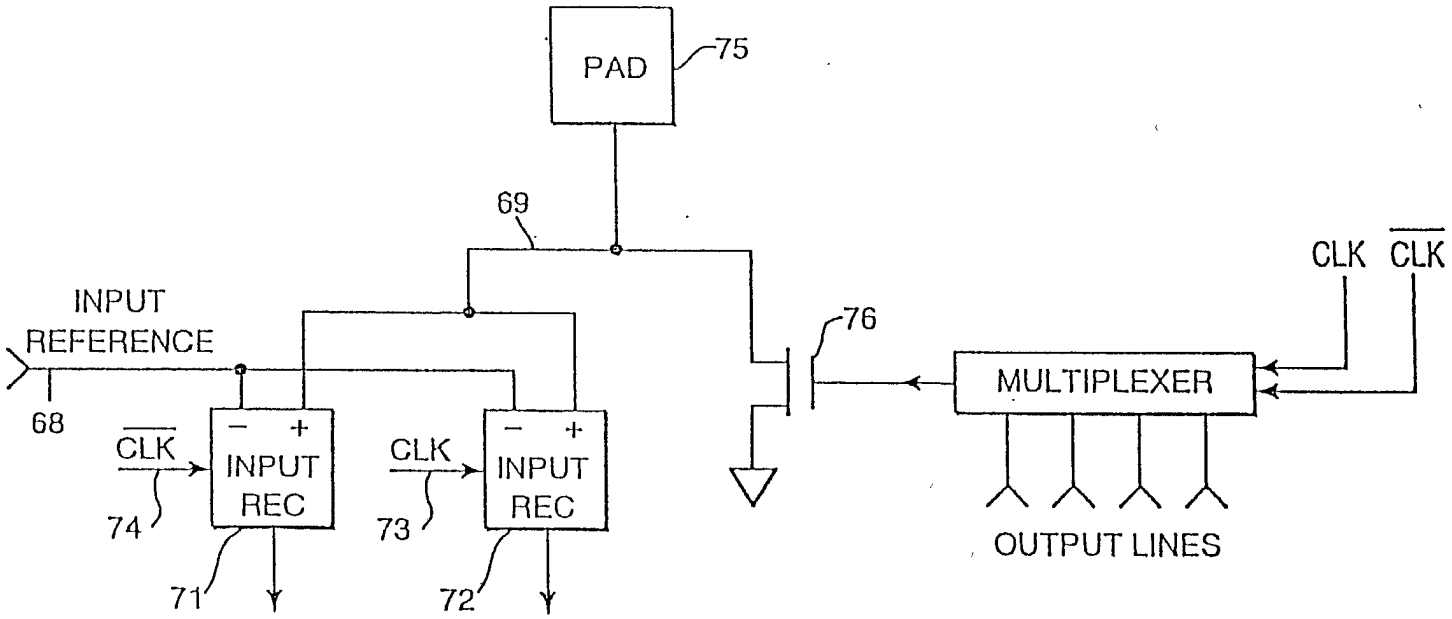

FIG_10

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No.: **RA001C13**)

In the Application of:	)
	)
FARMWALD ET AL.	)
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Serial No: Continuation of 09/835,263	)
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[signature]

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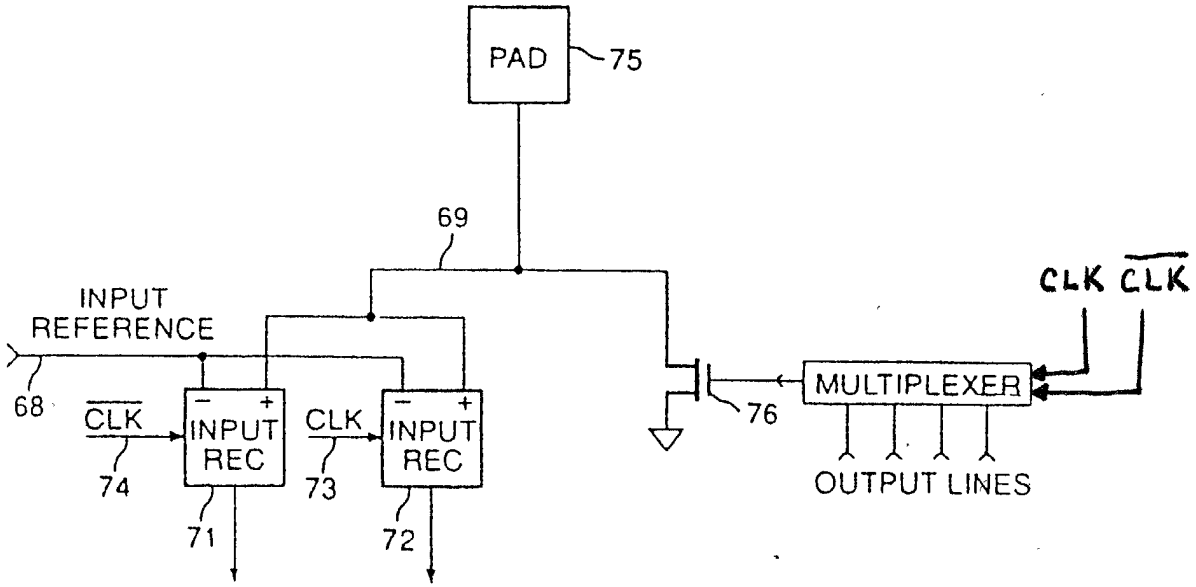

FIG. 10

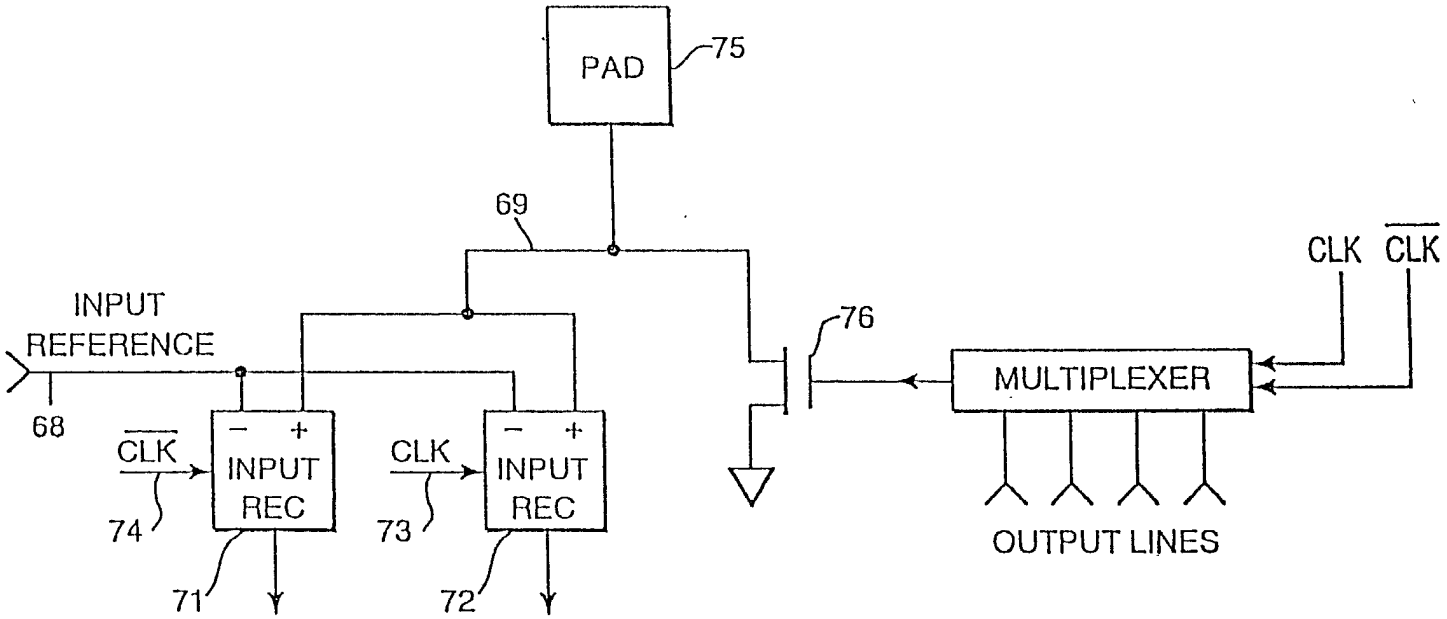

FIG_10